

What is claimed is:

- 1 1. A method for stabilizing data storage for a data-storage memory circuit in a
2 semiconductor device, the memory circuit including a thyristor device having a
3 capacitively-coupled control port and anode and cathode end portions, each end portion
4 including an emitter region and a base region, the capacitively-coupled control port
5 controlled to switch the thyristor device between a current passing mode and a current
6 blocking mode, the method comprising:
7 shunting low-level current at a first base region of a first one of the end portions.
- 1 2. The method of claim 1, wherein said first base region is doped n-type and wherein
2 shunting low-level current includes shunting low-level current between said first base
3 region and another node biased at a voltage at least equal to a voltage at which the
4 adjacent emitter region of said first end portion is biased.
- 1 3. The method of claim 1, wherein said first base region is doped p-type and wherein
2 shunting low-level current includes shunting low-level current between said first base
3 region and another node biased at a voltage not greater than a voltage at which the
4 adjacent emitter region of said first end portion is biased.
- 1 4. The method of claim 1, wherein shunting low-level current includes coupling a
2 shunt having a low resistance contact to the emitter region of said first end portion and
3 having a comparatively higher resistance contact to the first base region.

1 5. The method of claim 1, wherein shunting low-level current includes inhibiting the
2 thyristor device from inadvertently switching between current passing and current
3 blocking modes.

1 6. The method of claim 1, wherein shunting low-level current includes shunting
2 current that could otherwise cause the thyristor device to switch on inadvertently, were
3 the current not shunted.

1 7. The method of claim 1, further comprising capacitively coupling the control port
2 to a second base region at a second one of the end portions, wherein shunting current
3 includes shunting current at the first base region.

1 8. The method of claim 1, wherein shunting low-level current includes shunting
2 current between said first base region and an emitter region at the first one of the end
3 portions.

1 9. The method of claim 1, wherein shunting low-level current includes shunting
2 current between said first base region and a contact electrically coupled to an emitter
3 region adjacent to the first base region.

1 10. The method of claim 1, wherein shunting low-level current includes shunting
2 tunneling current to the base region.

1 11. The method of claim 1, wherein shunting current includes resistively coupling an
2 emitter and base region of the anode end portion.

1 12. The method of claim 1, wherein shunting current includes resistively coupling an
2 emitter and base region of the cathode end portion.

1 13. The method of claim 1, further comprising providing an intervening region
2 between the first base region and an emitter region at the first one of the end portions.

1 14. The method of claim 13, further comprising doping the intervening region to a
2 dopant concentration that is higher than the first base region.

1 15. The method of claim 13, wherein providing an intervening region includes
2 providing a depletion region in the intervening region and wherein shunting current
3 includes shunting current via the depletion region.

1 16. The method of claim 1, wherein the capacitively-coupled control port is adapted
2 to change the potential across a majority of a cross-section of a base region of the
3 thyristor.

1 17. A method for stabilizing data storage for a data-storage memory circuit in a
2 semiconductor device, the data-storage memory circuit including an array of thyristors,
3 each thyristor having a capacitively-coupled control port and anode and cathode end

4 portions, each end portion including an emitter region and a base region, the capacitively-
5 coupled control port being controlled to switch the thyristor between a current passing
6 mode and a current blocking mode, the array being adapted to store data for use in
7 conjunction with the semiconductor device, the method comprising:
8 shunting low-level current at a first base region of a first one of the end portions
9 of each thyristor.

1 18. A semiconductor device adapted for stabilizing data storage for a data-storage
2 memory circuit, the semiconductor device comprising:
3 a thyristor device having a capacitively-coupled control port and anode and
4 cathode end portions, each end portion including an emitter region and a base region, the
5 capacitively-coupled control port controlled to switch the thyristor device between a
6 current passing mode and a current blocking mode; and
7 means for shunting low-level current at a first base region of a first one of the end
8 portions.

1 19. A semiconductor device adapted for stabilizing data storage for a data-storage
2 memory circuit, the semiconductor device comprising:
3 a thyristor device having a capacitively-coupled control port and anode and
4 cathode end portions, each end portion including an emitter region and a base region, the
5 capacitively-coupled control port controlled to switch the thyristor device between a
6 current passing mode and a current blocking mode; and

7 a low-level current shunt adapted to shunt current at a first base region of a first
8 one of the end portions.

1 20. The semiconductor device of claim 19, wherein the low-level current shunt
2 includes a transistor having source and drain regions, one of the source and drain regions
3 being electrically coupled to the emitter region of an end portion of the thyristor device
4 and the other of the source and drain regions being electrically coupled to the base region
5 of the same end portion of the thyristor device, the transistor further having a gate
6 adapted to control the current flow between the source and drain regions.

1 21. The semiconductor device of claim 20, wherein the gate is electrically coupled to
2 a base region of another end portion of the thyristor device.

1 22. A method for manufacturing a semiconductor device adapted for stabilizing data
2 storage for a data-storage memory circuit, the method comprising:
3 forming a thyristor device having a capacitively-coupled control port and anode
4 and cathode end portions, each end portion including an emitter region and a base region,
5 the capacitively-coupled control port controlled to switch the thyristor device between a
6 current passing mode and a current blocking mode; and
7 forming a low-level current shunt adapted to shunt current at a first base region of
8 a first one of the end portions.

1 23. The method of claim 22, wherein forming a thyristor device includes doping the
2 first base region to n-type doping and wherein forming a low-level current shunt includes
3 forming the low-level current between the first base region and another node biased at a
4 voltage at least equal to a voltage at which the adjacent emitter region of the first end
5 portion is biased.

1 24. The method of claim 22, wherein forming a thyristor device includes doping the
2 first base region of a first end portion of the thyristor device to p-type doping and wherein
3 forming a low-level current shunt includes forming the low-level current shunt between
4 the first base region and another node biased at a voltage not greater than a voltage at
5 which the adjacent emitter region of the first end portion is biased.

1 25. The method of claim 22, wherein forming a low-level current shunt includes
2 coupling a shunt having a low resistance contact to the emitter region of the first end
3 portion of the thyristor device and having a comparatively higher resistance contact to the
4 first base region.

1 26. The method of claim 22, wherein forming a thyristor device includes forming the
2 control port capacitively coupled to a second base region at a second one of the end
3 portions.

- 1 27. The method of claim 22, wherein forming a low-level current shunt includes
2 forming the current shunt between the first base region and an emitter region at the first
3 one of the end portions.
- 1 28. The method of claim 22, further comprising forming an intervening region
2 between the first base region and an emitter region at the first one of the end portions.
- 1 29. The method of claim 28, further comprising doping the intervening region to a
2 dopant concentration that is higher than the dopant concentration of the first base region.
- 1 30. The method of claim 28, wherein forming an intervening region includes forming
2 a depletion region in the intervening region and wherein forming a current shunt includes
3 forming a current shunt adapted to shunt current via the depletion region.
- 1 31. The method of claim 22, wherein forming a thyristor device includes forming a
2 region having a low effective minority-carrier lifetime, the region at least including a
3 base-emitter junction of the first one of the end portions of the thyristor.
- 1 32. The method of claim 31, wherein forming a region having a low effective
2 minority-carrier lifetime includes forming a region having at least one of: poly-
3 crystalline, amorphous, or re-crystallized material.

1 33. The method of claim 32, wherein forming a region having a low effective
2 minority-carrier lifetime includes creating crystalline damage in the region.

1 34. The method of claim 31, wherein forming a region having a low effective carrier
2 lifetime includes introducing impurities that lower the lifetime into the region.